REMARKS

Claims 1, 7, 9-12, 15, 17-19, 21, 22, 25, 27, 91, 96-99, 101-103, 108-114 and 116-139 are currently pending, of which claims 1, 9, 15 and 129 are the pending independent claims. Claims 9, 15, 118, 129 and 133 are amended herein. Claims 4, 29, 30 and 115 were previously withdrawn and claims 2-3, 5-6, 8, 13-14, 16, 20, 23-24, 26, 28, 31-90, 92-95, 100, and 104-107 were previously cancelled. No new claims are added herein, and no claims are newly cancelled herein. No new matter is believed to have been introduced to the application by this paper. Reconsideration and further examination are respectfully requested.

Claim Rejections – 35 USC § 103

Claims 1, 7, 9-12, 15, 17-19, 21, 22, 25, 27, 91, 96-99, 101-103, 108-114 and 116-139 are rejected under 35 USC § 103(a) over Lin (U.S. Pat. No. 6,303,423) in view of Nakanishi (U.S. Pat. No. 6,921,980). Reconsideration and withdrawal of these rejections are respectfully requested.

Claim 1 is directed to an integrated circuit chip. The chip includes a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A second contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride. A first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening. A second opening in said passivation layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening. A power metal structure is over said passivation layer and on said first contact point. The power metal structure is connected to said first contact point through said first opening. The power metal structure comprises a copper layer. The power metal structure has a first region configured to be wirebonded thereto for connection made to a next level of packaging. A ground metal structure is over said passivation layer and on said second contact point. The ground metal structure is connected to said second contact point through said second opening. The ground metal structure comprises a copper layer. The ground metal structure has a second region configured to be wirebonded thereto for connection made to said next level of packaging. A capacitor is over said passivation layer, vertically over said power and

ground metal structures and vertically over said first contact point. A first solder joint is vertically over said first contact point and between a first terminal of said capacitor and said power metal structure, wherein said first solder joint connects said first terminal to said power metal structure. A second solder joint is between a second terminal of said capacitor and said ground metal structure, wherein said second solder joint connects said second terminal to said ground metal structure.

Claim 9 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, wherein said passivation layer comprises a nitride. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer. A capacitor is over said passivation layer and said second contact pad. A solder joint is between a terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad. A third contact pad between said solder joint and said second contact pad, wherein said third contact pad comprises electroplated copper, wherein a contact area between said third contact pad and said second contact pad is not vertically over said first contact point.

Claim 15 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein said passivation layer comprises a nitride, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening. A third contact pad over said semiconductor substrate, wherein said third contact pad is connected to said first contact point through said first opening and connected to said second contact pad, wherein said third contact pad has a region

that is configured to be wirebonded thereto for connection made to a next level of packaging and is not vertically over said first contact point. A first polymer layer over said passivation layer, wherein a second opening in said first polymer layer is over a second contact point of said second contact pad, and said second contact point is at a bottom of said second opening. A capacitor over said first polymer layer and said second contact point. A solder joint is between said second contact point and a terminal of said capacitor, wherein said solder joint connects said terminal to said second contact point.

Claim 129 is directed to an integrated circuit chip comprising a semiconductor substrate and a transistor in and on said semiconductor substrate. Multiple metal and dielectric layers are over said semiconductor substrate. A first contact pad is over said semiconductor substrate. A passivation layer is over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over a first contact point of said first contact pad, and said first contact point is at a bottom of said first opening, wherein said passivation layer comprises a nitride. A second contact pad is over said semiconductor substrate, wherein said second contact pad is connected to said first contact point through said first opening, wherein said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer. A capacitor is over said passivation layer and over said second contact pad. A solder joint between a terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad. A third contact pad is between said solder joint and said second contact pad, wherein said third contact pad is finished with a solder wettable material comprising gold, wherein a contact area between said third contact pad and said second contact pad is not vertically over said first contact point.

The applied references, either alone or in combination, are not seen to disclose or suggest the foregoing combination of features of each of independent Claims 1, 9, 15, and 129.

As a preliminary matter, Applicant notes that the Office Action states that "vertically over is different from directly vertically over – vertically over simply suggest above…[f]urther, as pointed out in previous office action, it does not appear that applicant's capacitor electrodes are all directly over the said first point (see for example right electrode 23 of Figure 3 which is not directly over 16); and applicant has not provided any argument against this." See Office Action, p. 21. Applicant respectfully submits that such an alleged issue regarding whether the

Specification adequately supports the claimed subject matter is not appropriately raised under an 35 USC § 103 "obviousness" rejection.

Even if, *in arguendo*, such an issue were properly raised, Applicants respectfully submit that one skilled in the art would know that the wording of "vertically" means "in a vertical direction." Accordingly, the wording of "vertically over said first contact point", as currently stated in Claim 1, means "over said first contact point in a vertical direction". Besides, Applicants further submit that the wording of "a capacitor .... vertically over said first contact point" does not only include the case that "all of the capacitor is vertically over said first contact point", but also includes the case that "a portion of the capacitor is vertically over said first contact point". Accordingly, in the present application, a capacitor 38 can be deemed vertically over a first contact point, connected to a power metal structure (left portion of element 23), at a bottom of a first opening in a passivation layer 18. Accordingly, the claimed subject matter that "a capacitor ... vertically over said first contact point", as currently claimed in Claim 1, is believed to be fully supported in the specification.

The Office Action also states that the Applicant did not address the combination of embodiments of Lin and Nakanishi in the previous response. See Office Action, p. 21. Applicant respectfully disagrees and respectfully notes that the last paragraph of p. 15 of the previous response addressed the combination of embodiments of Lin and Nakanishi. However, for the Examiner's convenience, Applicant has included below a rephrasing of this argument of the previous response.

As discussed in the previous response, in order to combine capacitor 54 of embodiments of Lin with Nakanishi's teaching of internal and external connections, Nakanishi's circuit design would need be applied to the device of embodiments of Lin. Applicant respectfully submits that the application of Nakanishi's circuit design to such a combination of embodiments of Lin and Nakanishi would result in the internal and external connections not functioning correctly. Therefore the proposed modification would render the embodiment of the applied reference unsatisfactory for its intended purpose. Applicant respectfully notes that if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. See *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

Accordingly, any combination of embodiments of Lin and Nakanishi's teaching of internal and external connections would include Nakanishi's circuit design. As such, the arrangement of the capacitor, the wiring trace, and the electrode pad of the combination would follow that of Nakanishi's discrete electronic component 48, Nakanishi's wiring trace 5, and Nakanishi's electrode pad 3. Thus, the electrode pad of the combination would be set in a peripheral area, as shown in Fig. 1a of Nakanishi. However, the electrode pad of the combination would not be set in a center region and under the capacitor as Nakanishi fails to teach, hint or suggest an advantage or motivation of setting a shortest path between Nakanishi's capacitor 8 and the IC metal of a chip, which makes Nakanishi's capacitor 8 able to provide power for the activated active circuit faster than the power would be provided through Nakanishi's wiring trace 25 to the activated active circuit. Thus, embodiments of Lin and Nakanishi, alone or in combination, fail to disclose or suggest the claimed subject matter of "a capacitor ..... vertically over said first contact point."

In view of the above, embodiments of Lin and Nakanishi, alone or in combination, fail to teach or suggest all of the elements of independent claims 1, 9, 15 and 129. For at least these reasons, independent claims 1, 9, 15 and 129 are believed to be allowable. Reconsideration and withdrawal of the rejections of independent claims 1, 9, 15 and 129 are respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the remarks set forth herein, Applicant submits that the application is in condition for allowance and respectfully requests a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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